

Get more visibility into your memory designs with the Tektronix DDR3/LPDDR3 Measurement and Analysis function (Opt. 6-DBDDR3) on the 6 Series MSO. The integration of the DDR3 software, oscilloscope, and high-performance analog probes lets you perform detailed, accurate amplitude, timing, and eye diagram measurements on your DDR designs to verify compliance with the Joint Electronic Device Engineering Council (JEDEC) electrical and timing specifications. The 12-bit analog-to-digital converters in the 6 Series MSO deliver high-precision measurement data with the lowest noise in the industry to let you achieve new levels of debugging efficiency and measurement reliability.

Key features

- Comprehensive DDR3 and LPDDR3 test coverage, supporting multiple memory standards.
- Intuitive user interface and test flow for easy DDR electrical validation.
- Automated read and write burst detection enables measurements over long record lengths.
- Measurements configure automatically for the selected memory specification and speed grade.
- Use the programmatic interface to automate memory tests and transfer measurement results for reports or further analysis.

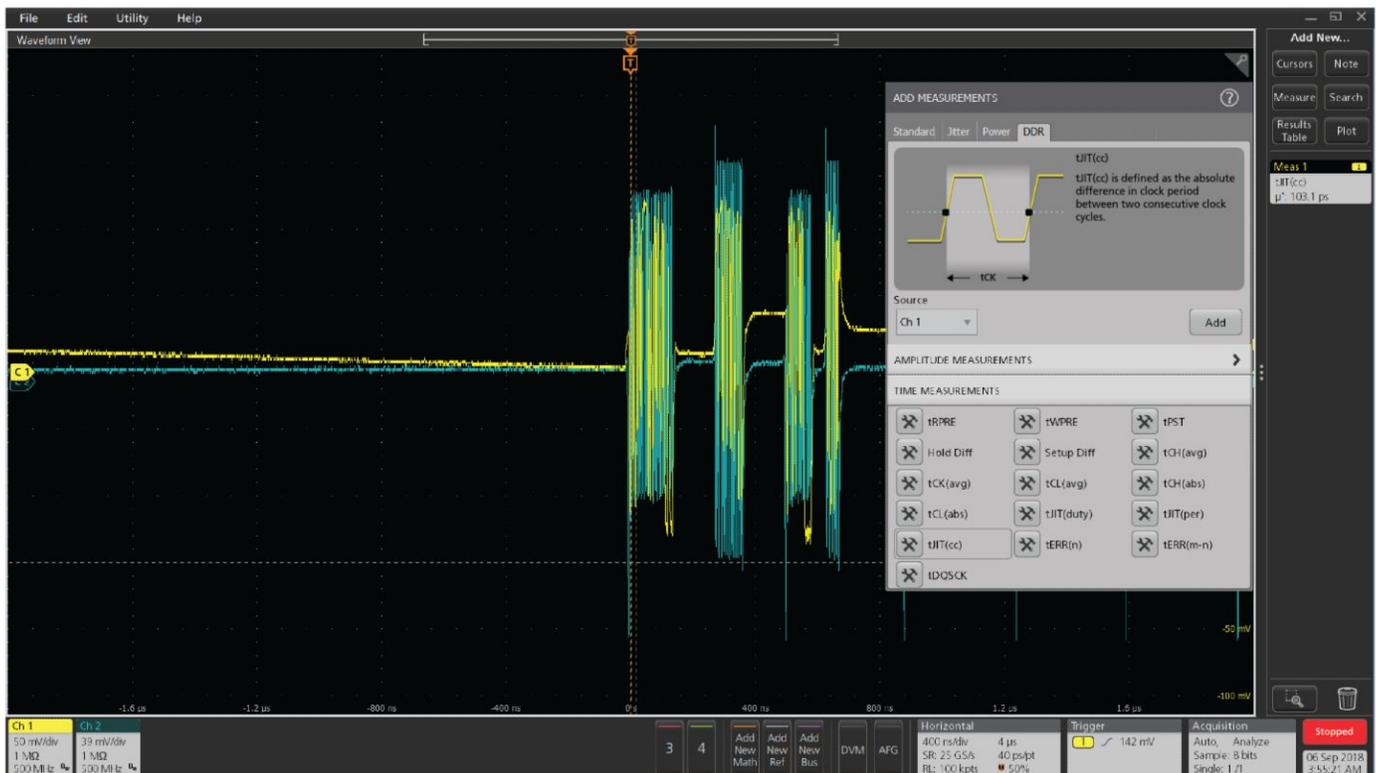
- Automated report generation saves measurements, test results, and plots in html or pdf file format.
- Quickly add, configure, and remove DDR measurements using the 6 Series MSO's pinch/swipe/zoom touch interface.
- Supports a wide range of interposers for different memory standards, along with best-in-class probes, to meet signal integrity requirements.

DDR3 debugging with Opt 6-DBDDR3

The 6-DBDDR3 solution lets you capture long records, automatically separate Read and Write bursts based on selected measurements, and perform measurements over multiple Read or Write bursts. You can run a defined number of measurements by programming a specific number of populations to acquire, or continuously run the measurements to perform statistical analysis.

The DDR measurements are available under the DDR tab of the Measure button. An included MOI (Method of Implementation) document provides instructions on how to set up the oscilloscope for specific measurements.

DDR3 electrical testing and timing analysis requires a 6 Series MSO oscilloscope with a minimum bandwidth of 8 GHz.



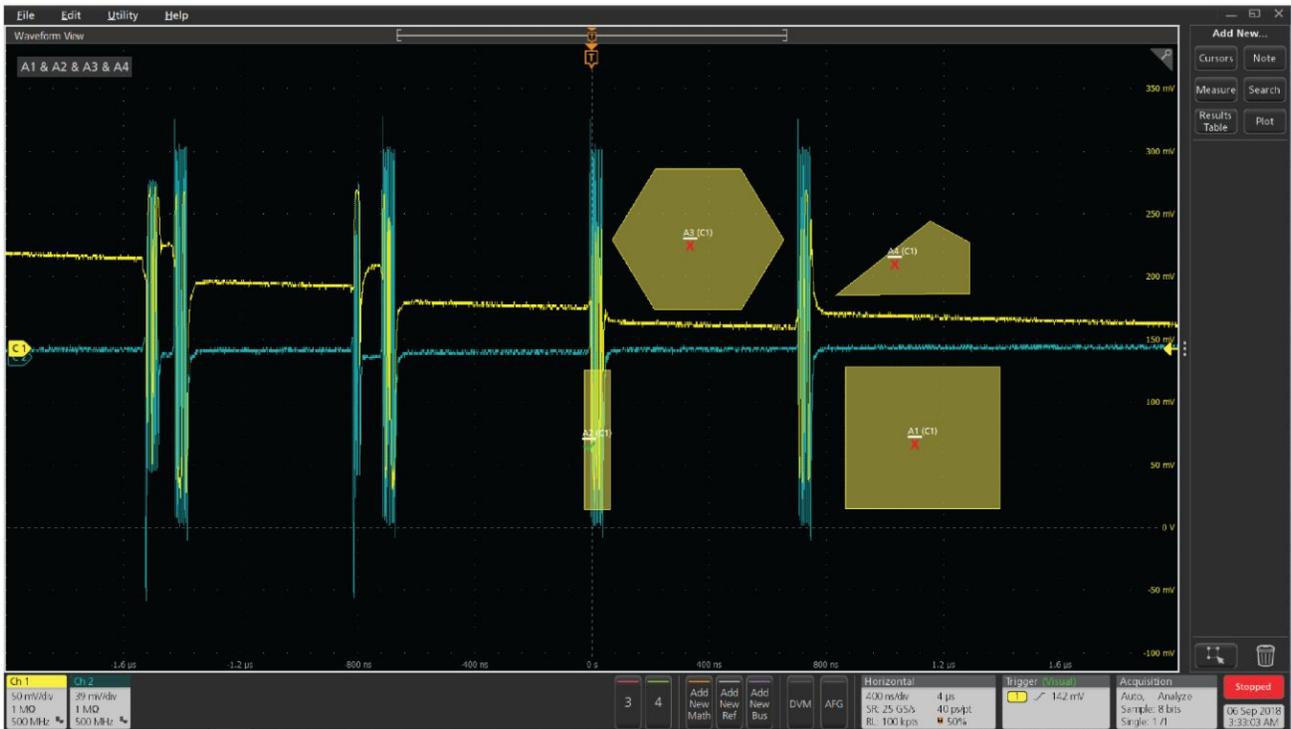
Just two screen taps are needed to open the DDR measurement menu.

Automated read and write burst detection

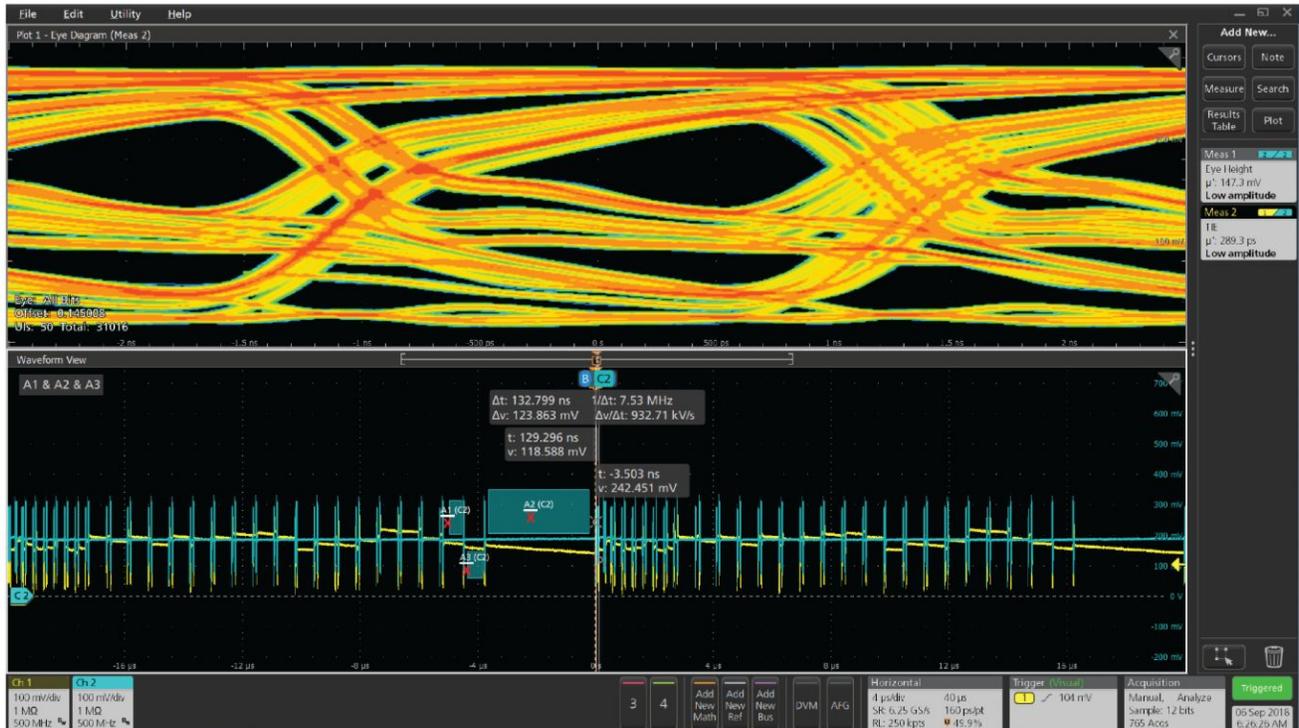
Some JEDEC conformance measurements require isolating the events of interest on the memory bus, such as read or write bursts.

For debug, it may be necessary to further isolate certain events by a particular rank or bank, or to isolate certain data patterns for analysis of signal-integrity issues such as data-dependent jitter, timing, or noise problems. The simplest way to achieve this is to use the DQS (Data Strobe signal) to identify the start of a read or write burst. For example, DDR3 always asserts DQS high at the start of a write, or low at the start of a read.

The Visual Trigger feature on the 6 Series MSO oscilloscope lets you further condition traditional triggers for more versatile DQS burst capture capability. Visual Trigger lets you create mask-like areas directly on the waveform display, where the boundaries of the areas help define trigger events for a DQS or Data Strobe signal.



Visual Trigger lets you add standard or user-specified areas to trigger the DDR3 waveform on specific trigger conditions.



An Eye Diagram of a DDR3 signal using Opt. 6-DJA measurement and Visual Trigger conditioning on the source waveform.

Making the complex easier

The JEDEC specifications for each memory technology specifies an array of conformance measurements. These measurements include clock jitter, setup and hold timing, transition voltages, signal overshoot and undershoot, slew rate and other electrical-quality tests. These tests are complex to measure using general-purpose tools.

Because the JEDEC-specified measurement methods require reference levels, pass/fail limits, and more, it is extremely valuable to have an application-specific measurement utility for DDR testing. Opt. 6-DBDDR3 is designed to correctly set up DDR measurements for specified devices. The broad set of measurements available in 6-DBDDR3 conforms to the JEDEC specifications. You can also customize settings to measure non-standard devices or system implementations.

Option 6-DBDDR3 works with option 6-DJA (Advanced Jitter Analysis) to provide Jitter and Eye Diagram Analysis Tools. These two utilities work together to create a powerful, flexible, and easy-to-use test suite for DDR testing and debug.

DDR search feature

The DDR search feature lets you search an entire waveform acquisition for specific signal conditions, such as DDR Read/Write, and mark the waveform where the conditions are met. In addition to using these marks for visual analysis, the oscilloscope can apply the marks as qualifiers for DDR-specific measurements, so that the measurements occur only on the appropriate portion of the data stream. The search algorithms in DDR search make use of the fact that DDR phase relationships are different for read and write bursts; DQ and DQS are in-phase for reads, and 90 degrees out-of-phase for writes. It also supports burst identification based on Chip Select (CS) signal and digital signals (Chip Select-CS, Row Access Strobe-RAS, Column Access Strobe-CAS, and Write Enable source-WE).

Easy test setup

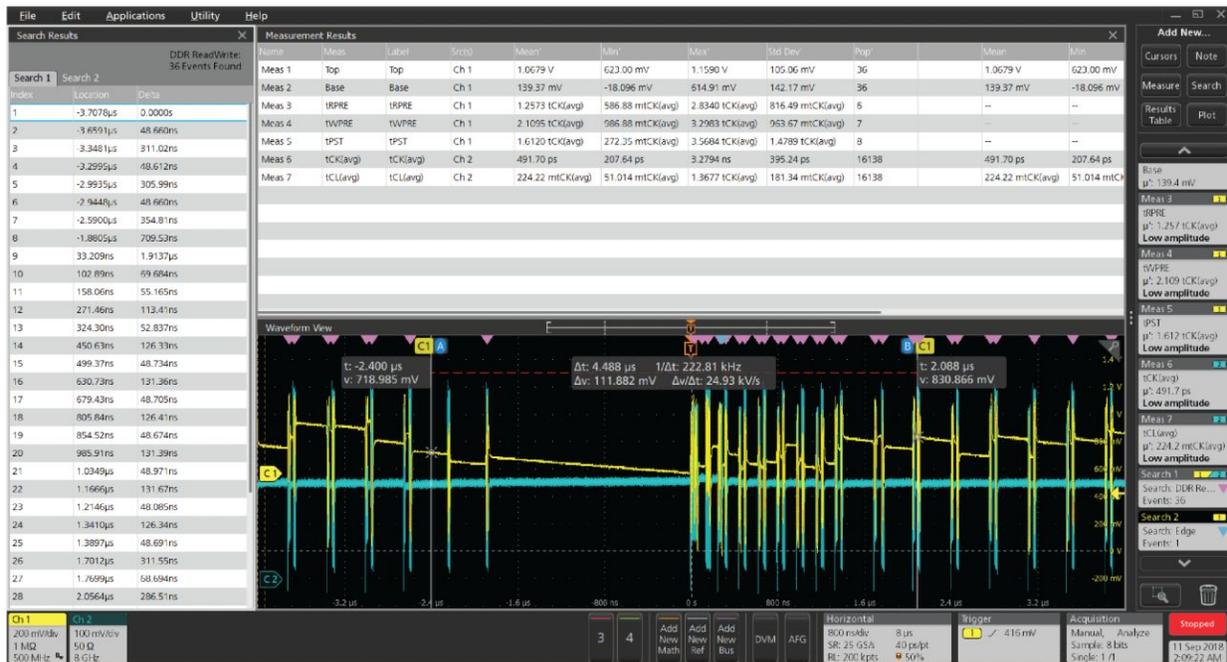
The first step is to select the DDR3 measurements to test. 6-DBDDR3 provides a comprehensive set of Clock, Read, Write, and Address/Command measurement setup files, accessible from the File > Recall > Setup menu. The files are grouped by memory type (DDR3 or LPDDR3).

Select the setup file for the measurement to take, tap Recall, and the oscilloscope activates all required source channels, adjusts the instrument settings, and adds all required measurements and searches to the Results bar. Connect probes from each oscilloscope channel to the source signal for that channel (labeled on the waveform for each channel).

Once the setup is complete and you select <Run> (or <Single>), the oscilloscope acquires the signals of interest, identifies and marks data bursts if needed, and takes the selected measurements. Using the default record length, the oscilloscope typically acquires around 1000 unit intervals, taking measurements on all valid edges in the acquisition.

Since the setup files are built with industry-standard measurement settings, you may need to modify the settings one time and save them if your test setup is different than the provided setup files.

You can add Search and Measurement Results tables to show the results in table format. The results tables display all measurement results with their statistical population, sources and other data. You can print a generated report, with an option to save the waveform data that is used to make the measurements.



Detailed results showing qualified bursts of a DDR3 signal.

Measurement Report **Teltronix**

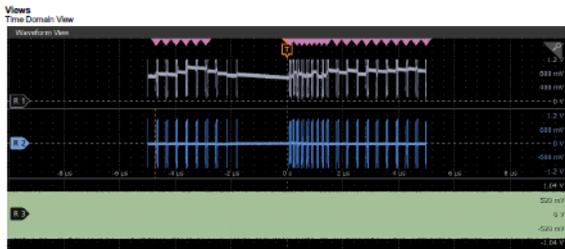
Tuesday September 11 2018 02:27:11

Setup Configuration

Scope Details			
Scope Model Number	Scope Serial Number	Firmware Version	Scope Calibration Status
ME094	GU100006	1.11.30	Fail

Measurement Result Details

Name	Meas	Sources	Meas1'	Meas1	Meas1'	Pk-Pk	Std Dev	Pref	Accum Meas	Accum Meas	Accum Pk-Pk	Accum Std Dev	Accum Pop
Meas1	Data Eye Height	Rut1 Rut2	572.0 mV	459.1 mV	949.4 mV	190.3 mV	40.29 mV	24	572.0 mV	459.1 mV	949.4 mV	190.3 mV	40.29 mV
Meas2	Data Eye Width	Rut1 Rut2	981.9 ps	819.2 ps	1,060 ns	240.4 ps	51.84 ps	24	981.9 ps	819.2 ps	1,060 ns	240.4 ps	51.84 ps
Meas3	V(OH)AC(DO)	Rut1	1.181 V	1,052 V	1,220 V	168.0 mV	26.27 mV	95	1.181 V	1,052 V	1,220 V	168.0 mV	26.27 mV
Meas4	V(OH)DC(DO)	Rut1	1.181 V	1,052 V	1,220 V	168.0 mV	26.27 mV	95	1.181 V	1,052 V	1,220 V	168.0 mV	26.27 mV
Meas5	V(OH)AC(DI)	Rut1	193.1 mV	4,000 mV	452.0 mV	448.0 mV	123.2 mV	95	193.1 mV	4,000 mV	452.0 mV	448.0 mV	123.2 mV
Meas6	V(OH)DC(DI)	Rut1	193.1 mV	4,000 mV	452.0 mV	448.0 mV	123.2 mV	95	193.1 mV	4,000 mV	452.0 mV	448.0 mV	123.2 mV
Meas7	IDPW-High	Rut1	2,308 ns	557.5 ps	10.14 ns	3,551 ns	1,785 ns	95	2,308 ns	557.5 ps	10.14 ns	3,551 ns	1,785 ns
Meas8	IDPW-Low	Rut1	2,291 ns	244.5 ps	9,329 ns	9,685 ns	1,726 ns	108	2,291 ns	244.5 ps	9,329 ns	9,685 ns	1,726 ns
Meas9	SRCoe-Full(DQ)	Rut1	5.674 Vns	3.972 Vns	678.0 mVns	9,004 Vns	1,736 Vns	98	5.674 Vns	3.972 Vns	678.0 mVns	9,004 Vns	1,736 Vns
Meas10	SRCoe-Full(DQ)	Rut1	3,483 Vns	1,059 Vns	5,052 Vns	3,993 Vns	961.1 mVns	106	3,483 Vns	1,059 Vns	5,052 Vns	3,993 Vns	961.1 mVns
Meas11	V(OH)A(C)	Rut2	910.7 mV	726.0 mV	990.0 mV	264.0 mV	60.66 mV	220	910.7 mV	726.0 mV	990.0 mV	264.0 mV	60.66 mV
Meas12	V(OH)A(C)	Rut2	845.9 mV	942.0 mV	762.0 mV	180.0 mV	36.86 mV	220	845.9 mV	942.0 mV	762.0 mV	180.0 mV	36.86 mV
Meas13	IDQSK-Diff	Rut3 Rut2	106.3 ns	-1.287 ns	1,227 ns	2,463 ns	712.1 ps	219	106.3 ns	-1.287 ns	1,227 ns	2,463 ns	712.1 ps
Meas14	IDQSQ-Diff	Rut3 Rut2	33.10 ns	452.8 ps	189.2 ps	942.0 ps	119.7 ps	218	33.10 ns	452.8 ps	189.2 ps	942.0 ps	119.7 ps
Meas15	IDVAC(DQS)	Rut2	1,110 ns	0.000 ns	1,287 ns	262.3 ps	464	1,100 ns	0.000 ns	1,287 ns	262.3 ps	464	
Meas16	ISH	Rut2 Rut1	1,303 ns	629.5 ps	1,478 ns	848.9 ps	168.0 ps	205	1,303 ns	629.5 ps	1,478 ns	848.9 ps	168.0 ps
Meas17	ISDR	Rut2	1,167 ns	301.8 ps	1,351 ns	1,040 ns	268.5 ps	244	1,167 ns	301.8 ps	1,351 ns	1,040 ns	268.5 ps
Meas18	ISDL	Rut2	1,238 ns	1,184 ns	1,319 ns	134.9 ps	26.68 ps	220	1,238 ns	1,184 ns	1,319 ns	134.9 ps	26.68 ps
Meas19	IRPRE	Rut2	1,065 ns	1,045 ns	1,007 ns	51.30 ns	11.04 ns	24	1,065 ns	1,045 ns	1,007 ns	51.30 ns	11.04 ns
Meas20	IRPST	Rut2	286.9 ns	151.3 ns	447.0 ns	205.7 ns	131.6 ns	24	286.9 ns	151.3 ns	447.0 ns	205.7 ns	131.6 ns
Meas21	SRCoe-Full(DQS)	Rut2	6.670 Vns	11.10 Vns	490.0 mVns	10.14 Vns	760.4 mVns	221	6.670 Vns	11.10 Vns	490.0 mVns	10.14 Vns	760.4 mVns
Meas22	SRCoe-Full(DQS)	Rut2	7,746 Vns	2,424 Vns	9,208 Vns	6,784 Vns	1,398 Vns	221	7,746 Vns	2,424 Vns	9,208 Vns	6,784 Vns	1,398 Vns



A detailed test report with setup details, measurement results and waveform image.

DDR3 main memory interposers

Gaining access to signal test points on a memory chip is a significant challenge in DDR testing. The JEDEC standards requires that measurements should be taken at the Ball Grid Array (BGA) ballouts of the memory component, connections that are very difficult to access.

Tektronix, in partnership with Nexus Technology¹, offers probing options such as BGA interposers that supports different memory devices in a variety of form factors. The interposer includes an embedded tip resistor placed close to the BGA pad. The DDR3 main memory is available in standard BGA component packages as well as dual-inline-memory-modules of DIMM and SODIMM.

Standard BGA packages are soldered directly to the printed circuit board (PCB) while modules comprise a series of packages in a standard PCB format with standard connections between the DIMM and the main board. Interposers are available for both component packages and DIMM and SODIMM modules.

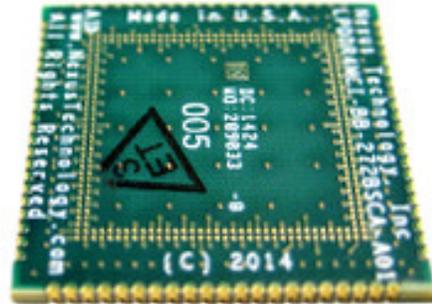
¹ For a detailed list of interposers, visit <http://www.nexustechnology.com>

Introduction of an interposer and an oscilloscope probe may change the characteristics of the signal. Apply de-embedding filters to remove the effect of the interposer and a probe in the signal path to get an accurate representation of the signal at the probe point.

EdgeProbe Interposer

The Nexus Technology's patented EdgeProbe™ interposer is available for DDR3, LPDDR3, and other new memory products. It has a small mechanical footprint as the probe points are on the edge of the interposer. The probes can attach directly to the target device to provide access to the clock, command bus, data, strobe, and address signals.

The EdgeProbe design removes mechanical clearance issues as the interposers are the size of the memory components. Embedded resistors within the interposers place the oscilloscope probe tip resistor extremely close to the BGA pad, by providing an integrated oscilloscope probe on all the signals.

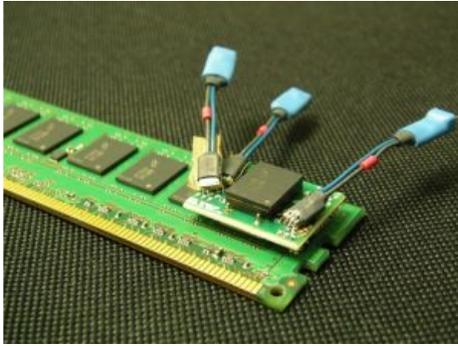


EdgeProbe interposer

Socketed Interposer

A socketed interposer typically provides access to all component signals and elevates the interposer above adjacent components for mechanical clearance. This solution offers a custom socket that is installed on the target and has an interposer that is installed by pressing it into the socket. Retention is designed into the solution since the interposer can be removed by pulling an unsecured interposer from the target socket.

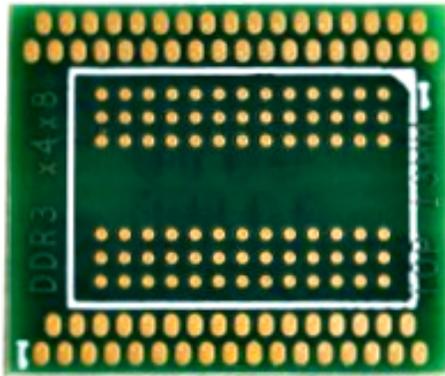
The interposer can have the memory component soldered directly to it or optionally have a socket on the interposer. The socket on the interposer allows for memory components to be manually inserted and removed to easily evaluate different vendor memory components. When testing is completed, the interposer can be removed and the memory device inserted directly into the custom socket on the target, removing the effect of the interposer.



Socketed interposer.

Direct Attach Interposer

The direct attach interposer enables probing of all signals and is installed directly onto the target. The target must have mechanical clearance for the interposer. The use of the direct attach interposers is common for Package on Package (PoP) components.



Direct Attach interposer.

Technology	Package / Form factor
DDR3	Socketed – 78 Ball / 96 Ball Edge Probe – 78 Ball / 96 Ball Solder-down – 78 Ball / 96 Ball DIMM and SODIMM Interposer for MSO
LPDDR3	Socketed – 216 Ball / 211 Ball Solder-down – 178 Ball / 211 Ball

TDP7700 series TriMode probes for DDR3 measurements

The Tektronix TDP7700 Series TriMode probes are designed to meet DDR3 measurement challenges. The TDP7700 works with the 6 Series MSO, with full AC calibration of the probe and tip's signal path, to provide the highest probe fidelity available for real-time oscilloscopes. The innovative new probe design uses SiGe technology to provide the bandwidth and fidelity needed today and in the future.

TriMode probing lets one probe setup take differential, single ended, and common mode measurements accurately, increasing your efficiency. This unique capability lets you switch between differential, single ended and common mode measurements on the oscilloscope, without moving the probe's connection point.

A key TDP7700 connectivity innovation is using solder-down probe tips with the probe's input buffer mounted only a few millimeters from the tip. This approach provides unmatched usability for connecting to DDR3 circuits.



The TDP7708 probe with high impedance inputs and TriMode capability reduces the number of probes needed to take DDR3 measurements.

Other TDP7700 Series probe characteristics include:

- Excellent step response and low insertion loss up to 20 GHz
- Low-DUT loading with 100 kΩ (DC) and 0.4 pF (AC) performance
- High Common-Mode Rejection Ratio (CMRR)
- Low noise

TLP058 FlexChannel® logic probe for digital measurements

The 6 Series MSO provides digital channel capabilities to perform full protocol analysis of the entire memory bus. The TLP058 FlexChannel® logic probe connects the Tektronix 6 Series MSO to digital buses and signals on the device under test (DUT). The probe contains 8 data channels and connects the TLP058 logic probe to any FlexChannel oscilloscope input channel.



The TLP058 provides high performance digital inputs.



Configuring DDR3 digital measurements using TLP058 probes.

Specifications

- **Timing measurements**

- **tRPRE** measures the width of the Read burst preamble. This is measured from the exit of tristate to the first driving edge of the differential strobe.
- **tWPRE** measures the width of the Write burst preamble. It is measured from the exit of tristate to the first driving edge of the differential strobe.
- **tPST** measures the width of Read or Write burst postamble. It is measured from the last falling edge crossing the mid reference level to the start of an undriven state (as measured by a rising trend per JEDEC specification).
- **Hold Diff** measures the elapsed time between the designated edge of the single-ended waveform and the designated edge of a differential waveform. The measurement uses the closest single-ended waveform edge to the differential waveform edge that falls within the range limits.
- **Setup Diff** measures the elapsed time between the designated edge of a single-ended waveform and when the differential waveform crosses its own voltage reference level. The measurement uses the closest single-ended waveform edge to the differential waveform edge that falls within the range limits.
- **tCH(avg)** measures the average high pulse width calculated across a sliding 200 cycle window of consecutive high pulses.
- **tCK(avg)** measures the average clock period across a sliding 200-cycle window.
- **tCL(avg)** measures the average low pulse width calculated across a sliding 200 cycle window of consecutive low pulses.
- **tCH(abs)** measures the high pulse width of the differential clock signal. It is the amount of time the waveform remains above the mid reference voltage level.
- **tCL(abs)** measures the low pulse width of the differential clock signal. It is the amount of time the waveform remains below the mid reference voltage level.
- **tJIT(duty)** measures the largest elapsed time between tCH and tCH(avg) or tCL and tCL(avg) for a 200-cycle window.
- **tJIT(per)** measures the largest elapsed time between tCK and tCK(avg) for a 200-cycle sliding window.
- **tJIT(cc)** measures the absolute difference in clock period between two consecutive clock cycles.
- **tERR(n)** measures the cumulative error across multiple consecutive cycles from tCK(avg). It measures the time difference between the sum of clock period for a 200-cycle window to n times tCK(avg).
- **tERR(m-n)** measures the cumulative error across multiple consecutive cycles from tCK(avg). It measures the time difference between the sum of clock periods for a 200-cycle window to n times tCK(avg).
- **tDQSCK** measures the strobe output access time from differential clock. It is measured between the rising edge of clock before or after the differential strobe Read preamble time. The edge locations are determined by the mid-reference voltage levels.
- **tCMD-CMD** measures the elapsed time between two logic states.
- **tCKSRE** measures the valid clock cycles required after Self Refresh Entry (SRE) command. Changing the input clock frequency or the supply voltage is permissible only after tCKSRE time when the SRE command is registered.
- **tCKSRX** measures the valid clock cycles required before the Self Refresh Exit (SRX) command. Changing the input clock frequency or the supply voltage is permissible provided the new clock frequency or supply voltage is stable for the tCKSRX time prior to SRX command.

- **Amplitude measurements**

- **AOS** measures the total area of the signal above the specified reference level.
- **AUS** measures the total area of the signal below the specified reference level.
- **Vix(ac)** measures the differential input cross-point voltage measured from the actual crossover voltage and its complement signal to a designated reference voltage. This is measured on a single-ended signal.
- **AOS Per tCK** measures the total area of the signal that crosses the specified reference level calculated over consecutive periods. It is applicable to clock and address/command waveforms only.
- **AUS Per tCK** measures the total area of the signal that crosses the specified reference level calculated over consecutive periods. It is applicable to clock and address/command waveforms only.
- **AOS Per UI** measures the total area of the signal that crosses the specified reference level calculated over consecutive unit intervals. It is applicable to data and data strobe waveforms only.
- **AUS Per UI** measures the total area of the signal that crosses the specified reference level calculated over consecutive unit intervals. It is applicable to data and data strobe waveforms only.

Additional details

Details	DDR3	LPDDR3
Speed (MT/s)	800, 1066, 1333, 1600, 1866, and 2133	333, 800, 1066, 1200, 1333, 1466, 1600, 1866 and 2133
Max slew rate	10 V/ns	8 V/ns
Typical V swing	1 V	0.6 V
20-80 risetime	60 ps	45 ps
Report	HTML and PDF format	
Source support	Live analog signals, reference waveforms, and math waveforms	
De-embedding support	Filter file using math subsystem	

Ordering information

Models

Product	Options	Supported instruments
New Instrument order option	6-DBDDR3	6 Series MSO (MSO64)
Product upgrade option	SUP6-DBDDR3	
Floating license	SUP6-DBDDR3-FL	6 Series MSO (MSO64) Floating licenses are transferrable from any 6 Series oscilloscope to any other 6 Series oscilloscope, for use of one instrument at a time.

Additional information about DDR analysis is available at <https://www.tek.com/ddr-test-validation-and-debug>.

Recommended probes and accessories

Recommended probes

Accessory type	Quantity
TDP7708 Tri-mode probe with P77STFLXA adapters	Two probes are required for testing a DUT with DQ and DQS. Three probes are required for testing a DUT with DQ, DQS and clock.
TLP058	One probe is required for probing CS, RAS, CAS, and WE lines.

Recommended test fixtures

Accessory type	Vendor
DDR3: x4, x8, 16 socketed, solder-down and direct attach interposers	Sold through Tektronix and Nexus Technologies ²
LPDDR3: BGA and PoP interposers	



Tektronix is registered to ISO 9001 and ISO 14001 by SRI Quality System Registrar.



Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.



Product Area Assessed: The planning, design/development and manufacture of electronic Test and Measurement instruments.

² Contact your local Tektronix representative for details.

ASEAN / Australasia (65) 6356 3900
Belgium 00800 2255 4835*
Central East Europe and the Baltics +41 52 675 3777
Finland +41 52 675 3777
Hong Kong 400 820 5835
Japan 81 (3) 6714 3086
Middle East, Asia, and North Africa +41 52 675 3777
People's Republic of China 400 820 5835
Republic of Korea +822 6917 5084, 822 6917 5080
Spain 00800 2255 4835*
Taiwan 886 (2) 2656 6688

Austria 00800 2255 4835*
Brazil +55 (11) 3759 7627
Central Europe & Greece +41 52 675 3777
France 00800 2255 4835*
India 000 800 650 1835
Luxembourg +41 52 675 3777
The Netherlands 00800 2255 4835*
Poland +41 52 675 3777
Russia & CIS +7 (495) 6647564
Sweden 00800 2255 4835*
United Kingdom & Ireland 00800 2255 4835*

Balkans, Israel, South Africa and other ISE Countries +41 52 675 3777
Canada 1 800 833 9200
Denmark +45 80 88 1401
Germany 00800 2255 4835*
Italy 00800 2255 4835*
Mexico, Central/South America & Caribbean 52 (55) 56 04 50 90
Norway 800 16098
Portugal 80 08 12370
South Africa +41 52 675 3777
Switzerland 00800 2255 4835*
USA 1 800 833 9200

* European toll-free number. If not accessible, call: +41 52 675 3777

For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit www.tek.com.

Copyright © Tektronix, Inc. All rights reserved. Tektronix products are covered by U.S. and foreign patents, issued and pending. Information in this publication supersedes that in all previously published material. Specification and price change privileges reserved. TEKTRONIX and TEK are registered trademarks of Tektronix, Inc. All other trade names referenced are the service marks, trademarks, or registered trademarks of their respective companies.

